

EXHIBIT 1

ARM® CoreTile Express A15×2 A7×3

Cortex®-A15_A7 MPCore (V2P-CA15_A7)

Technical Reference Manual

ARM®

ARM CoreTile Express A15x2 A7x3

Technical Reference Manual

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Release Information

The following changes have been made to this book.

Change history			
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The information in this document is final, that is for a developed product.

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About this book

This book is for the CoreTile Express A15×2 A7×3 daughterboard.

Intended audience

This document is written for experienced hardware and software developers to aid the development of ARM-based products using the CoreTile Express A15×2 A7×3 daughterboard with the Motherboard Express µATX as part of a development system.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the CoreTile Express A15×2 A7×3 daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the daughterboard.

Appendix A *Signal Descriptions*

Read this for a description of the signals present on the daughterboard.

Appendix B *HDLCD controller*

Read this for a description of the HDLCD controller in the Cortex-A15_A7 test chip.

Appendix C *Electrical Specifications*

Read this for a description of the electrical specifications of the daughterboard.

Appendix D *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, <http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html>.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page ix
- *Timing diagrams* on page ix
- *Signals* on page x.

Chapter 1

Introduction

This chapter provides an introduction to the CoreTile Express A15×2 A7×3 daughterboard. It contains the following sections:

- *About the CoreTile Express A15×2 A7×3 daughterboard* on page 1-2
- *Precautions* on page 1-4.

1.1 About the CoreTile Express A15×2 A7×3 daughterboard

The CoreTile Express A15×2 A7×3 daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA) that use the *Advanced eXtensible Interface* (AXI) or custom logic for use with ARM cores.

You can use the CoreTile Express A15×2 A7×3 daughterboard to create prototype systems.

Note

You can use the CoreTile Express A15×2 A7×3 daughterboard with a Motherboard Express µATX See [System interconnect signals](#) on page 2-6 for information about interconnection.

You can also use the CoreTile Express daughterboard with a custom-design motherboard. See [ARM® Programmer Module \(V2M-CP1\)](#).

The daughterboard includes the following features:

- Cortex-A15_A7 MPCore test chip, with NEON™, that is, the advanced *Single Instruction Multiple Data* (SIMD) extension, and *Floating Point Unit* (FPU), that contains a dual-core A15 cluster operating at 1GHz and a triple-core A7 cluster operating at 800MHz.
- Cortex-A15_A7 MPCore test chip internal AXI subsystem operating at 500MHz.
- Simple configuration with V2M-P1 motherboard:
 - Configuration EEPROM.
 - Daughterboard Configuration Controller.
- Nine programmable oscillators.
- 2GB of daughterboard DDR2 32-bit memory operating at 400MHz.
- *High Definition LCD* (HDLCD) controller that supports up to 1920×1080p video at 60Hz, 165MHz pixel clock.
- CoreSight software debug and 32-bit trace ports.
- HDRX header with one multiplexed AMBA AXI master bus port that connects to the other daughterboard site on the V2M-P1 motherboard.
- HDRY header with four buses to the motherboard:
 - *Static Memory Bus* (SMB).
 - *MultiMedia Bus* (MMB).
 - *Configuration Bus* (CB).
 - *System Bus* (SB).
- *Power Supply Units* (PSUs) for the Cortex-A15_A7 test chip and DDR2 memory.
- Core voltage control and current, temperature, and power monitoring.
- On-board energy meter.

Note

The Cortex-A15_A7 test chip does not support TrustZone®.

[Figure 1-1 on page 1-3](#) shows the layout of the daughterboard:

2.2 Cortex-A15_A7 MPCore test chip

Figure 2-2 shows the main components of the test chip.

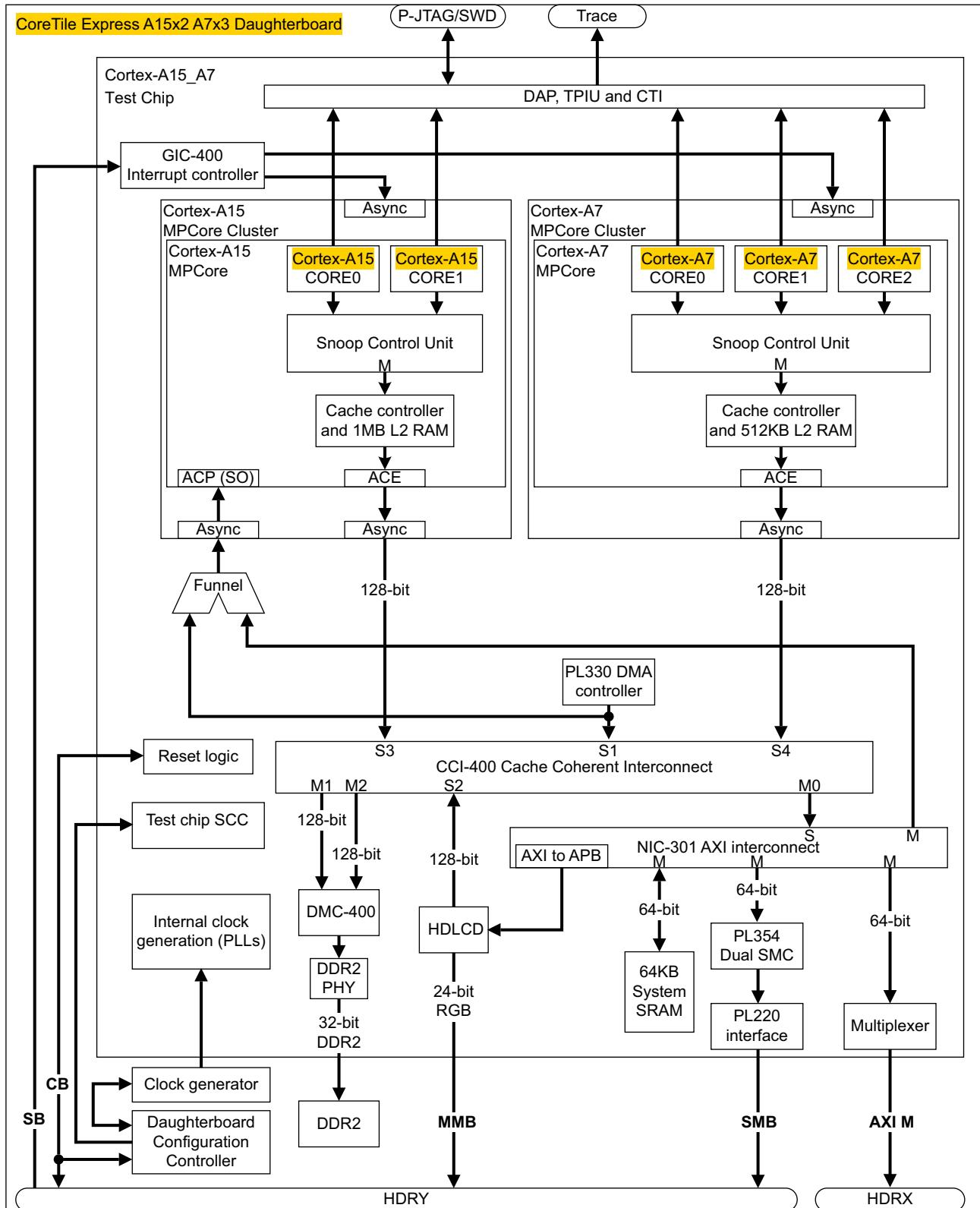


Figure 2-2 Top-level view of the Cortex-A15_A7 MPCore test chip components

Note

Bus lines with single-headed arrows indicate the direction of control, not the direction of data flow. That is, each arrow points from bus master to bus slave.

Cortex-A15_A7 MPCore test chip

The test chip includes the following components and interfaces:

- **Cortex-A15 dual-core** cluster operating at 1GHz:
 - Version r2p1.
 - 32KB I/D cache.
 - NEON and *Floating Point Unit* (FPU).
 - ACP port.
 - 1MB L2 cache.
 - Dual *Program Flow Trace Macrocell* (PTM).
- **Cortex-A7 triple-core** cluster operating at 800MHz:
 - Version r0p1.
 - 32KB I/D cache.
 - NEON and FPU.
 - 512KB L2 cache.
 - Dual *Embedded Trace Macrocell* (ETM).
- NIC-301 AXI interconnect operating at 500MHz.
- CCI-400 cache coherent interconnect operating at 500MHz that provides cache-coherency between the two clusters.
- DMC-400 32-bit *Double Data Rate 2* (DDR2) *Dynamic Memory Controller* (DMC) interface to the onboard 2GB DDR2 memory.
- PL354 32-bit SMB controller (SMC). This connects to the motherboard peripherals.
- PL330 *Direct Memory Access* (DMA) controller.
- 24-bit HDLCD video controller that drives the MMB to the MUXFPGA on the V2M-P1 Motherboard Express.
- Multiplexed 64-bit AXI master interface.
- 64KB of local on-chip SRAM.
- CoreSight debug and trace interface to the onboard connectors:
 - PTM for each Cortex-A15 core.
 - ETM for each Cortex-A7 core.
 - 16KB ETB.
 - DAP.
 - *Trace Port Interface Unit* (TPIU) for real-time trace data.
 - JTAG interface for debug.
- *Serial Configuration Controller* (SCC) interface:
 - Interfaces to the Daughterboard Configuration Controller.
 - Configures the test chip *Phase-Locked Loops* (PLLs) during power up or reset.
- Interrupts interface:
 - Connects interrupt signals from the V2M-P1 motherboard to the *Generic Interrupt Controller* (GIC) in the test chip.

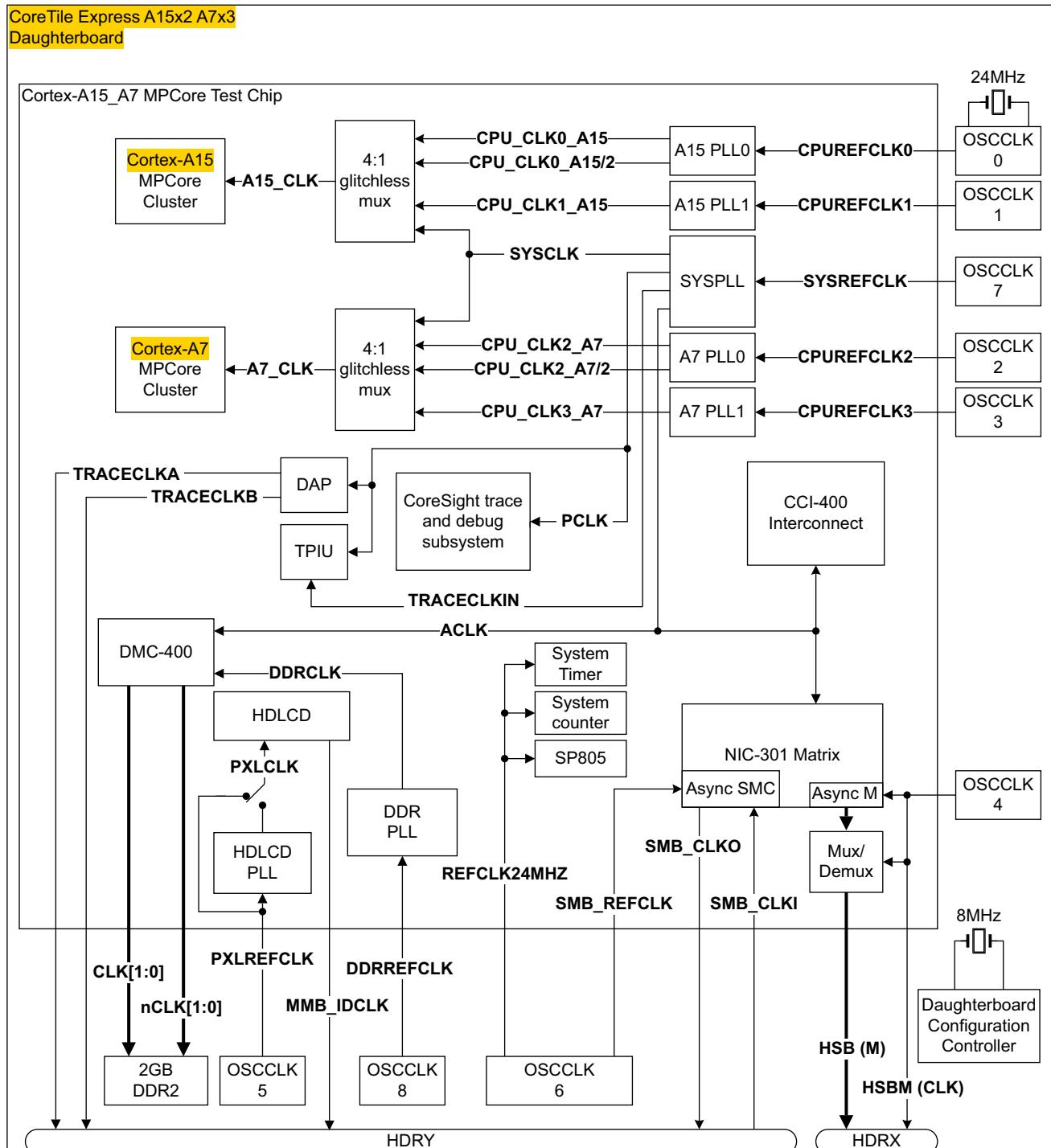
**Figure 2-10 CoreTile Express A15x2 A7x3 daughterboard clocks**

Figure 2-10 shows the default inputs for the PLLs. You can independently select **SYSREFCLK** as the inputs to any or all of:

- A15 PLL0.
- A15 PLL1.
- A7 PLL0.
- A7 PLL1.
- HDLCD PLL.

- DDR PLL.

See [Test chip SCC Register 11 on page 3-27](#).

CPU_CLK0_A15 is the default source for **A15_CLK**.

CPU_CLK2_A7 is the default source for **A7_CLK**.

You can use the 4-way glitchless multiplexers to select any of the four inputs as the sources for **A15_CLK** and **A7_CLK**. See [Test chip SCC Register 11 on page 3-27](#).

When you write to the SCC registers to change the sources for the MPCore clocks, you can monitor when the change takes effect by reading the clock status register. See [Test chip SCC Register 12 on page 3-30](#).

You can select the polarity of **MMB_IDCLK** relative to **PXLREFCLK**. It can be either in phase with **PXLREFCLK** or inverted. See [Polarities Register bit assignments on page B-17](#).

You can also use the SCC registers to exercise other options, for example, to select *External Bypass* to bypass the PLL and drive the reference clock into the design.

— Note —

The configuration process bypasses the HDLCD PLL by default.

ARM does not recommend that you select non-default options for the other PLLs and [Figure 2-10 on page 2-26](#) does not show these options. See [Test chip SCC Register 11 on page 3-27](#) and [Test chip SCC Registers 13, 15, 17, 19, 23, and 25 PLL control registers on page 3-31](#).

The MCC and Daughterboard Configuration Controller use the board.txt configuration file for the daughterboard to set the frequency of the daughterboard clock generators and to configure the SCC registers on power-up or reset. You can also adjust the daughterboard clocks during run-time by using the motherboard SYS_CFG register interface.

For more information see:

- [Power-up configuration and resets on page 2-10](#).
- [Versatile™ Express Configuration Technical Reference Manual](#) for an example board.txt file.
- [Motherboard Express µATX Technical Reference Manual](#).

2.7.2 Daughterboard programmable clock generators

This section describes the daughterboard clock generators and the clocks that the test chip generates from them to drive the on-chip systems.

The following SCC registers control the PLLs, clock divider blocks and PLL input select multiplexers:

- [Test chip SCC Register 11 on page 3-27](#)
- [Test chip SCC Register 12 on page 3-30](#)
- [Test chip SCC Registers 13, 15, 17, 19, 23, and 25 PLL control registers on page 3-31](#)
- [Test chip SCC Registers 14, 16, 18, 22, 24 and 26 PLL value registers on page 3-33](#).